



**NEOS TECHNOLOGIES**

A Gooch & Housego Company

OPERATING MANUAL  
**DIGITALLY CONTROLLED  
FREQUENCY SYNTHESIZER**

MODEL NUMBER:

**64020-200-2ADMDFS-A**

**DOCUMENT NUMBER: 51A18839**

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## **SECTION I INSPECTION**

Examine the shipping carton for damage. If the shipping carton or packing material is damaged it should be kept for the carrier's inspection. . Notify the carrier and NEOS Technologies. Check the contents of the shipment for completeness, mechanical damage, and then test the equipment electronically. Operating procedures are contained in Section IX. If the contents are incomplete, or the equipment does not pass the electrical testing please notify NEOS Technologies.

If there is any problem with the use of this equipment, or if the equipment fails to function as expected contact NEOS Technologies, do not try to trouble shoot or repair this equipment. Consult with a NEOS service engineer. If the equipment needs repair or replacement, contact NEOS Technologies, Inc for a Return Authorization Number.

## SECTION II

### GENERAL DESCRIPTION

The 64010-200-2AMDFS-A is a digitally controlled frequency synthesizer. It is designed to supply a RF output of up to 2 watts of RF energy into an Acousto-Optic Device having a nominal impedance of  $50 \Omega$  or a  $50 \Omega$  load. The system requires +28 VDC and +3.3 VDC power input; A TTL level 30 bit binary word to set the frequency for the synthesizer; and 0 to +1 volt analog input for setting power level. There also is a reference output for the synthesizer that is nominally 10 dBm. See the driver Acceptance Test Report for performance data.

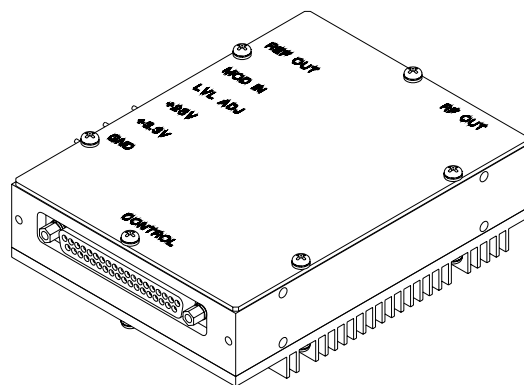
The "Frequency Select" digital 30 bit binary word signal is input through a 37 pin D sub connector to the synthesizer. In addition to the 30 "Frequency Select" data input lines, there are three other control lines:

The "Latch" function is used to keep the current output frequency from changing while a new input word is being generated. For best operation, the new word should be formed while the latch is "HIGH", the latch signal brought "Low" for 50 ns to load in the data, and then returned to the "HIGH" state. The latch function requires an active TTL "HIGH" as the latch input is pulled low through a  $4.7 \text{ k}\Omega$  resistor.

The "Digital Modulation" function disables the output of the driver. This function requires a TTL active low as the input is pulled high internally via a  $4.7 \text{ k}\Omega$  resistor.

The "Reset" is used to disable the output of the driver and clear the stored frequency information. This function requires a TTL active high as the input is pulled LOW via a  $1 \text{ k}\Omega$  resistor.

**64010-200-2AMDFS-A**



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**SECTION III  
SPECIFICATION**

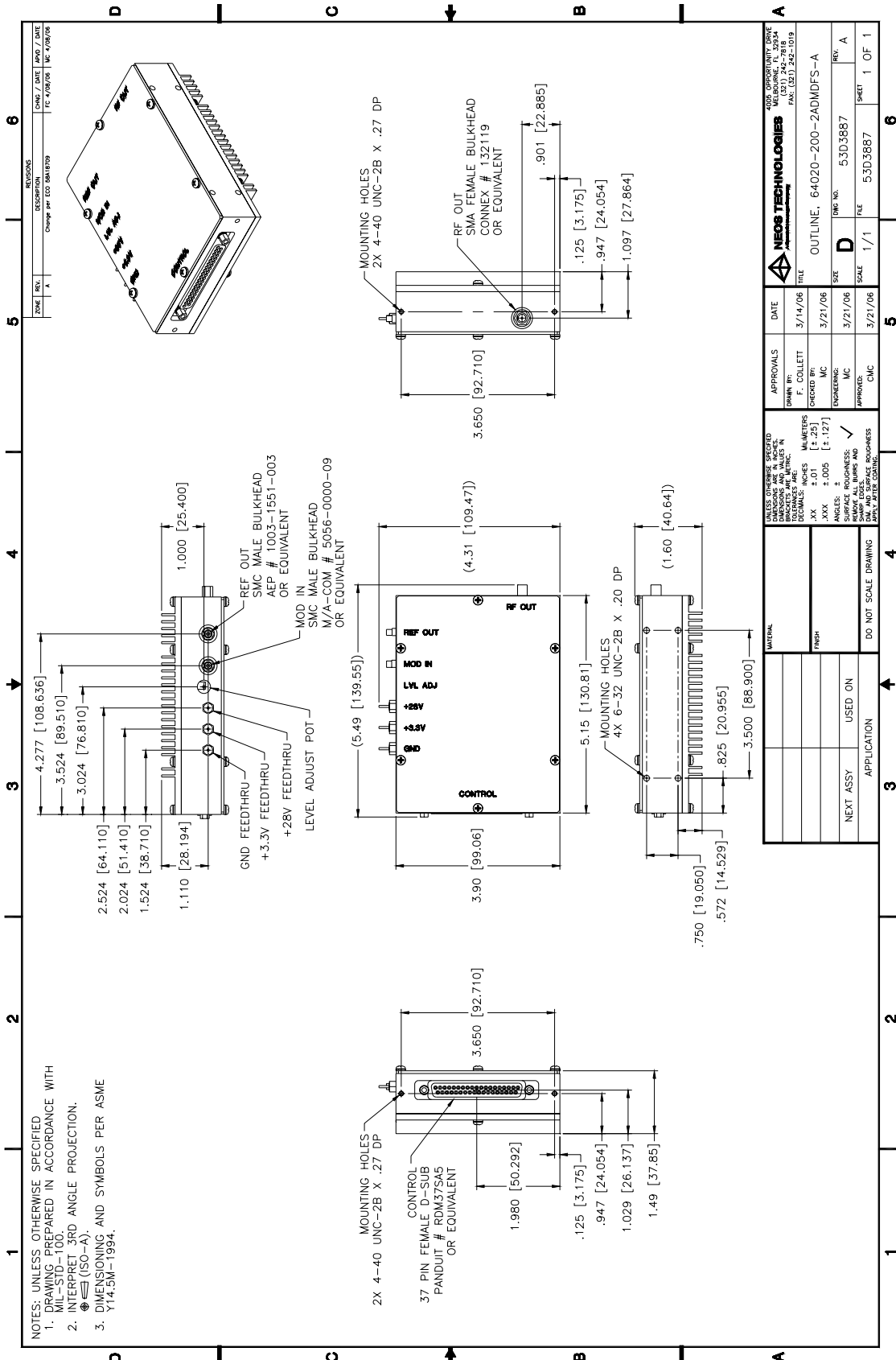
**MODEL NUMBER: 64020-200-2ADMDFS-A**

<u>PARAMETER</u>	<u>SPECIFICATION</u>
Bandwidth	20 – 200 MHz Typical
Clock Frequency	1000 MHz
Step Size	<1 Hz with 30 Bits input
Power Out	2 watts Typical
Rise and Fall Time	20 ns
Harmonic Distortion	2nd <-20 dB 3rd <-15 dB
Extinction Ratio	Digital 30 dB Analog 40 dB
Output Impedance	50 Ω Nominal
Applied Power	+28 VDC @ 1.0 amp max. +3.3 VDC @ 1.0 amps max.
External Modulation ("Mod In")	0 to +1 volt analog, +1 volt = full RF Power output
"Frequency Select" Control	TTL 30 bit binary word
"Latch" Control	The “Latch” function is used to keep the current output frequency from changing while a new input word is being generated. TTL active HIGH on pin 16.
"Digital Modulation" Control	The “Digital Modulation” function disables the output of the driver. This function requires a TTL active low as the input is pulled high internally via a 4.7KΩ resistor. A TTL active low on pin 35.
"Reset" Control	The “Reset” is used to disable the output of the driver and clear the stored frequency information. This function requires a TTL active high as the input is pulled LOW via. a 1 KΩ resistor. A TTL active HIGH on pin 17.

Output Frequency Versus Input Data  $F_{out} = \frac{(F_{osc})(K_{10})}{2^n}$

Where:  $K_{10}$  = input word in decimal notation  
 $F_{osc}$  = Clock Frequency  
 $n = 31$

# SECTION IV OUTLINE DRAWING



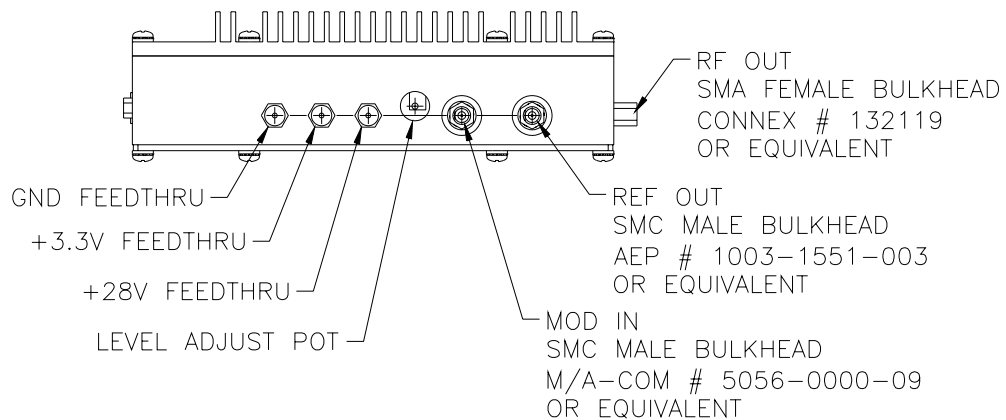
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## SECTION V

### CONTROLS AND CONNECTIONS

- A. "RF Out" SMA Female The output of the driver supplies two Watts of RF energy into the Acousto-Optical Beam Deflector or 50 Ω.
- B. "Mod In" SMC Female This port accepts an analog modulation voltage between "0" and +1volt, +1 volt is full RF output.
- C. "Reference" SMC Female This port output a reference signal from the un-modulated that is 10dBm nominal.
- D. "Frequency Select" 37 PIN Sub D Connector This port accepts a 30 bit TTL word to set the frequency of the oscillator and the "Digital Modulation", "Reset", and a "Latch" control inputs. See page 8 for pinout.
- E. +28 Volt Power Input Stud +28 VDC @ 1.0 amp max
- F. +3.3 Volt Power Input Stud +3.3 VDC @ 1.0 amps max
- G. GND Stud Ground return connection
- H. RF Output Power Level Adjustment Pot

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SYNTHESIZER 64020-200-2ADMDFS-A  
 "FREQUENCY SELECT" PIN OUT  
 37-PIN MALE D-SUB CONNECTOR

<u>PIN</u>			<u>PIN</u>		
1	FS <sub>0</sub>	LSB	20	FS <sub>1</sub>	
2	FS <sub>2</sub>		21	FS <sub>3</sub>	
3	FS <sub>4</sub>		22	FS <sub>5</sub>	
4	FS <sub>6</sub>		23	FS <sub>7</sub>	
5	FS <sub>8</sub>		24	FS <sub>9</sub>	
6	FS <sub>10</sub>		25	FS <sub>11</sub>	
7	FS <sub>12</sub>		26	FS <sub>13</sub>	
8	FS <sub>14</sub>		27	FS <sub>15</sub>	
9	FS <sub>16</sub>		28	FS <sub>17</sub>	
10	FS <sub>18</sub>		29	FS <sub>19</sub>	
11	FS <sub>20</sub>		30	FS <sub>21</sub>	
12	FS <sub>22</sub>		31	FS <sub>23</sub>	
13	FS <sub>24</sub>		32	FS <sub>25</sub>	
14	FS <sub>26</sub>		33	FS <sub>27</sub>	
15	FS <sub>28</sub>		34	FS <sub>29</sub>	MSB
16	Latch, Active High		35	Digital Modulation, Active High	
17	Master Reset, Active High		36	N/C	
18	N/C		37	N/C	
19	Ground				

$$\text{Control Word } K_{10} = \frac{F_{\text{OUT (Hz)}}(2^{31})}{F_{\text{OSC (Hz)}} \text{ in decimal notation}}$$

## SECTION VI

### CONTROL WORD CALCULATIONS

The output frequency and step size is a function of the clock rate and the "frequency select" data. The output frequency can be calculated from the formula:

$$f_{out} = \frac{(f_c)(k_{10})}{2^n}$$

Where:  $f_c$  = clock frequency in Hz

$k_{10}$  = input word in decimal notation

$n = 31$  \*See note below.

The minimum output frequency and step size are given by:

$$f_{min} = \frac{f_c}{2^n}$$

An example of setting the frequency:

Clock frequency =  $1000 \times 10^6$  Hz

Desired output frequency =  $30.00 \times 10^6$  Hz

$$K_{10} = \frac{f_{OUT(Hz)}(2^{31})}{f_{OSC(Hz)}}$$

$$K_{10} = \frac{30 \times 10^6 (2^{31})}{(1000 \times 10^6)}$$

$$K_{10} = 64424509.44 \text{ decimal}$$

Convert  $K_{10}$  to Binary

∨ LSB - pin1

$K_B = 000011110101110000101000111101$  -Setting for binary word input to "FREQUENCY SELECT" 37 pin D-SUB CONNECTOR

\*Note: This system only uses 30 bits to set the frequency output from the driver. The accumulator inside the chip is 31 bit, so use  $2^{31}$  in your calculations for precision.

The "Latch" function is TTL active HIGH and is located on pin 16. The "Latch" function is used to keep the current output frequency from changing while a new input word is being generated. TTL active HIGH on pin 16.

The "Reset" is used to disable the output of the driver and clear the stored frequency information. This function requires a TTL active high as the input is pulled LOW via a 1 K $\Omega$  resistor. A TTL active HIGH on pin 17.

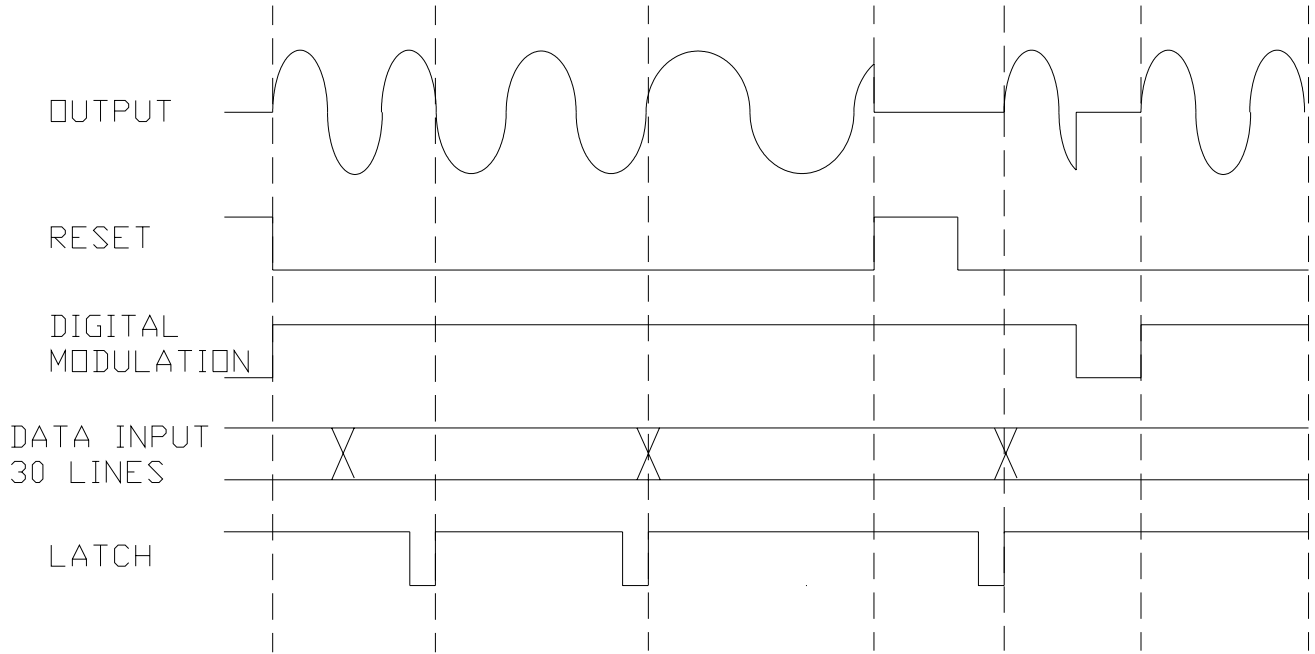
## SECTION VII

### CIRCUIT DESCRIPTION

The NEOS 64020-200-2ADMDFS-A is a digital frequency synthesizer consist of a DFS circuit with a 30 bit binary word "Frequency Select" input control and a 1GHz clock, a manual output power level adjustment, a "Digital" and "Analog" Mod in input to control the output power level, a pre-amplifier stage, a output power amplifier stage, and a un-modulated "reference" signal output. In addition to the 30 "Frequency Select" data input lines, there are three other control lines. The "Latch", which when a TTL active HIGH is applied to pin 16 of the 37-pin male D sub connector, will hold the frequency at the last word sent to the driver prior to setting the latch HIGH. The "Digital Modulation" function disables the output of the driver when a TTL low is applied on pin 35. This function is pulled HIGH internally via a 4.7K $\Omega$  resistor. The "Reset" is used to disable the output of the driver and clear the stored frequency information. This function requires a TTL active high as the input is pulled LOW via. a 1 K $\Omega$  resistor. A TTL active HIGH on pin 17. See the signal timing diagram on the next page.

### SECTION VIII TIMING DIAGRAM

TIMING AND WAVEFORM DIAGRAM  
FOR FREQUENCY SYNTHESIZER



45A15240A

## SECTION IX

### OPERATING PROCEDURES

#### TESTING:

- A. Connect the "RF out" to a 50  $\Omega$  load capable of dissipating 2 watts with a 50  $\Omega$  cable.
- B. Connect a 30 bit digital control cable to the "Frequency Select" (37 pin D sub connectors). See page 8 for pin out for LSB TO MSB. Note: No signal is required on the "Latch", "Reset", or "Digital Modulation" control lines for the driver to output RF.
- C. Connect +1VDC to the "Mod In" Analog input (SMC connector). (1VDC = full RF output). DO NOT EXCEED 1VDC.
- D. Connect the "Reference Out" output to your frequency counter.
- E. Connect +28 volts to the +28 volt stud and return to the ground lug.
- F. Connect +3.3 volts to the +3.3 volt stud and return to the ground lug.
- G. Turn on the Power Supplies.
- H. With the +1 volt on the "Mod In" analog input, apply a 30 bit digital word to the "Frequency Select" (37 pin D Sub Connector). Test the frequency output vs. word input. See calculations on page 9.
- I. Set the word to the operating frequency or center frequency of the AO device, (See the AO Acceptance Test Report), adjust the driver output power level control for the power required for maximum diffraction efficiency of the AO device or to a power which does not exceed the maximum allowed for the AO device. **Warning: The driver will output up to 2 watts of RF power. Do not exceed the maximum allowed for the AOBD device or damage will occur.** If damage results due to overpowering the AO device, the warranty will be void.
- J. Test rise time of the RF by applying an appropriate signal to the "Mod In" analog input. Do not apply the RF output directly to an oscilloscope as damage will occur. Use an attenuator capable of dissipating 2 watts.
- K. Test the RF output for other parameters as listed on the specifications for this module. See the Acceptance Test Report for data.

**OPERATION: Typical for AOBDs or AOTFs.**

- A. Attach the AO device to the RF output of the driver with a 50  $\Omega$  cable.
- B. With the driver turned on, and +1 volt on the analog "Mod In", apply the necessary word to the "Frequency Select" port to output the operating frequency or center frequency for the AO device. This will set the frequency to produce an output beam from the AO device to be at the center of the optical path. For some AO devices there is an angular offset for the output beam. See AO Acceptance Test Report for information on operating frequency, bandwidth, and output angle vs. frequency information.
- C. **Follow the instructions in the AO device manual to align and adjust the AO device as required in your optical system.**
- D. Apply a TTL LOW signal to the "Latch" control line to keep the current frequency before selecting a new frequency. Apply the necessary signals to the "Frequency Select" port as desired to select a new output frequency. Then, apply a TTL High signal to the "Latch" control line to switch to the new frequency. See timing and control diagram in section VIII.
- F. Apply the needed signals to the "Reset", and "Digital Modulation" control lines to control the "blinking" if needed.
- G. If power leveling is required to achieve "field flatness" for an AOBD or AOTF, then apply the necessary words to the "Frequency Select" port as desired and apply the needed analog signal to the "Mod In" analog port as each word is input to output the needed power to compensate for AO's "field flatness". **Do not exceed the maximum allowable power for the AO as damage may occur. Note:** It is necessary to check the diffraction efficiency at each end of the AO devices bandwidth and adjust the Bragg angle for the AO device to the flattest output field before trying to compensate for RF drive power as any change in Bragg angle will affect the diffraction efficiency of the AO across the output field.